Model Predictive Control of a Cascaded H-bridge Multi-level StatCom

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***Abstract*—A multi-level H-bridge StatCom inherently contains redundancy in the available switching states. This paper develops a Model Predictive Control (MPC) scheme which is able to exploit this redundancy to optimise three competing objectives. The scheme can simultaneously balance the H-bridge capacitor voltages, provide excellent current reference tracking and optimise converter switching losses. A variation in modulation scheme, consisting of a hybrid of traditional MPC and PWM strategies, is also described. Simulation and experimental results are presented that confirm the correct operation of the control and modulation strategies. Comparison with traditional control and modulation schemes is provided in terms of the key performance indicators associated with multi-level H-bridge StatComs.**

I. Introduction

Multi-level Static Compensators (StatComs) are increasingly being implemented as cascaded H-bridge converters. The main reasons for the choice of this topology are: (i) the number of components used in the construction of each level scales linearly; (ii) various control algorithms exist which control the balancing of capacitor voltages for high level numbers; (iii) the H-bridges form a modular section of each phase leg which makes construction and maintenance easier; and (iv) the level number can be increased to allow direct connection of the converter to medium voltages which avoids the lossy and expensive connection transformer. Throughout the remainder of this paper the acronym H-StatCom will be used to refer to a multi-level StatCom implemented with cascaded H-bridges.

Traditional techniques for controlling the firing of the H-bridges in the individual phase legs use either multiple triangular carrier waves for each of the H-bridges [1], or precomputed firing angles for the bridges to implement Selective Harmonic Elimination (SHE) [2]. The control and modulation techniques used in this paper are based on the instantaneous power concept [3], [4] coupled with MPC [5] current control and symmetrical PWM [6], [7]. The main advantage of this approach is that it operates in the stationary reference frame, and the control at any instant of time is dependent only on values measured or computed at that time. The MPC nature of the control loops means that their bandwidth is very high. In addition the calculations are numerically simple and ideal for digital implementation. Furthermore, it is relatively simple to incorporate a very high performance capacitor voltage balancing algorithm into the MPC scheme. This algorithm uses a logic based cost function to evenly share the leg cluster voltage across the individual H-bridge capacitors. A separate control loop keeps the leg cluster voltages at a setpoint value [8]. This technique avoids some of the control loop interaction problems present in other strategies [9].

This paper extends previous work by implementing an MPC scheme for a H-StatCom. The control approach allows simultaneous optimisation of current control, voltage balancing and switching losses, and is realisable with readily available digital hardware. The MPC algorithm is able to exploit the available redundancy in the switching states for a 9-bridge/leg H-StatCom to trade-off between the voltage balancing and switch utilisation characteristics, while still achieving excellent reference current tracking performance.

Remark 1: MPC is an excellent control technique when saturation and other non-linearities are present in a control problem. The control strategy allows the generation of a near optimal control output whilst implicitly accounting for the non-linearities. The other advantage of the approach is that it allows trade-offs between competing control objectives to be elegantly handled within the control generation. It is this aspect of MPC that is being exploited in this paper. ■

II. Algorithm Structure

Fig. 1 is a block diagram of the control algorithm. Most of the blocks in this figure have been discussed previously [8], except for the new MPC block. Note that the original deadbeat control block has not been removed because the MPC algorithm uses

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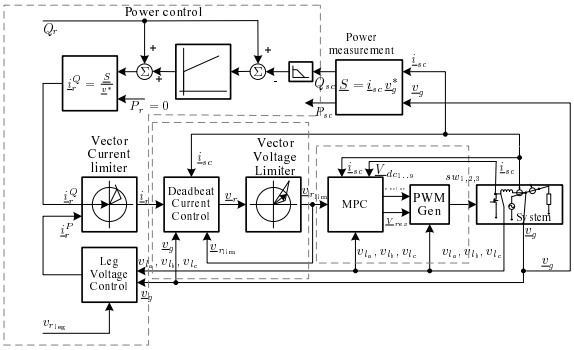

Figure 1. Block diagram of the H-StatCom control with MPC.

the deadbeat control equations to form the basis for the model of the current reference tracking. The MPC block integrates the deadbeat control equations with a logic based penalisation related to the voltage balancing and switch utilisation. This is the basis of a cost function which selects the voltage vector to be applied in the next control interval.

The information passed to the PWM block includes the chosen voltage vector and the residual voltage error between the voltage determined by the deadbeat controller and the voltage chosen by the MPC controller. The PWM block uses the residual error to calculate the required duty cycle to be applied to an appropriate bridge, using symmetrical PWM. The most appropriate bridge is determined using the same logic based model which is used within the MPC. This is explained in more detail in Section III.

In typical finite state MPC applications there is one cost function which uses a system model to calculate an error for the particular vector being evaluated. For a three phase 9-bridge H-StatCom there are more than one billion possible switching states that can be applied. Evaluating the error for such a large number of vectors requires significant computational effort which is unachievable with the available hardware. The computational effort can be reduced by constraining the applied vector to be within a subspace of the possible solution set [6]. However when optimising the voltage balancing, the number of vectors which need to be evaluated can exceed 15 million, depending on the magnitude of the voltage vector which needs to be applied and the number of capacitors needed to create this vector. In [6] the capacitor voltages are assumed to be ideal, therefore only the number of bridges that are switched in is of any relevance. When voltage balancing is included within the cost function, not only the number of bridges but also which particular bridges are switched becomes important. This means a greater number of vectors must be evaluated to find an acceptable solution. The authors have implemented three cost functions to reduce computation time. By evaluating the possible switching states on a per phase basis the total switching combinations reduce to 3069. It is possible to evaluate the cost function for these switching states by utilising the processing power of the Pentium IV PC used as the system's control hardware. This approach does not limit the performance of the MPC scheme when optimising the current control, voltage balancing and switch utilisation as these characteristics have no coupling between the phases. In Section IV a comparison is provided in terms of the performance, between the MPC scheme developed in this paper and that developed by Cortes et al. in [6].

III. Algorithm Implementation

To implement the MPC algorithm a model of the system must first be developed. The discrete time model of the load is developed from the governing equations between voltage and current for resistive and inductive elements.

$$i_{k+1} = \frac{T}{L}\left(V_{\text{applied}} - i_k\left(R - \frac{L}{T}\right)\right)$$

$$V_{\text{applied}} = V_{dc} \bullet S_i$$

where T is the length of the k^{th} control interval in seconds, i_k is the current at the beginning of the k^{th} control interval, i_{k+1} is the current at the end of the k^{th} control interval and V_{applied} is the voltage vector generated by the switching states S_i, for the interval $k \rightarrow k+1$ i.e the k^{th} interval.

Once the model has been developed the component of the cost function to control the current can be defined as:

$$g\left(t_k\right) = \left|i_{\text{ref},k+1} - i_{\text{vec},k+1}\right| \tag{1}$$

where i_{ref} is the desired current at the end of the k^{th} control interval and i_{vec} is the current at the end of the same control interval assuming the evaluated vector is applied.

The prediction horizon for the MPC algorithm used in this paper is one. This means that the vector chosen for each control interval is only based on the events which occur in the models within one control cycle. There are advantages in increasing the prediction horizon. The main advantage is the reduction of switching transitions, which will be the subject of a future paper. The form of the cost function can also be varied. In (1) the projected error in the current is penalised linearly. Other forms of penalisation such as those shown in (2) and (3) can also be used.

$$g\left(t_k\right) = \left|i_{\text{ref},k+1} - i_{\text{vec},k+1}\right|^2 \tag{2}$$

$$g\left(t_k\right) = \frac{1}{T}\int^{T}\left[i\left(t\right)_{\mathrm{ref},k+1} - i\left(t\right)_{\mathrm{vec},k+1}\right]dt \qquad (3)$$

In applying the form of (2), the cost function ascribes an over proportional penalisation for larger errors. This form can further reduce the current ripple, but possibly at the expense of other control objectives. The form of (3) takes into account the multiple sampled current values during the switching interval and not just the end points. This provides better current tracking performance in the average sense. The three forms described here do not produce vastly different current tracking performance in most converter applications due to sufficiently high switching frequencies [5]. However, for H-StatCom systems these three basic forms can be used to provide extra flexibility for the multi objective control algorithm.

Having defined the model for the current tracking, the MPC cost function can be expanded to include errors associated with voltage balancing and switch utilisation. The form of the cost function becomes:

$$\begin{aligned}\text{error} = {} & \alpha_1\left(i_{\mathrm{ref},k+1} - i_{\mathrm{vec},k+1}\right) \\ & + \alpha_2\left(V_{\mathrm{cap,ideal}} \otimes V_{\mathrm{vec}}\right) + \alpha_3\left(SW_{\mathrm{transitions}}\right) \qquad (4)\end{aligned}$$

where $V_{\mathrm{cap,ideal}}$ is an ideal voltage vector, V_{vec} is the evaluated vector and $SW_{\mathrm{transitions}}$ is the number of transitions from the previous applied vector to the evaluated vector. The $\otimes$ symbol is used to denote a comparison operation between two vectors which have been sorted based on the H-bridge capacitor voltages.

The MPC algorithm is implemented with the following steps:

1) Determine the applied stack voltage for the bridges being evaluated. This voltage is used to extrapolate the current at the end of the next control interval assuming that this voltage vector is applied. An error value is obtained by subtracting the result from the current reference at the end of the next control interval. This gives a measure of how close the evaluated voltage vector will move the H-StatCom current to the reference waveform;
2) The vector is compared to an ideal vector in which each capacitor is assigned an index. The index of each capacitor is determined by the voltage on the capacitor at the time of evaluation. If the stack is charging then the ideal vector will begin with the capacitor with the lowest voltage and end with the capacitor with the highest voltage. The converse is true if the stack is discharging. The closer the vector under investigation is to the ideal vector the lower the associated error;
3) The vector under investigation is compared to the previous switching combination which was applied. An error value is obtained by counting the number of switching transitions which would occur if this vector was applied in the next interval;
4) Finally these three error components are scaled by a different scaling factor before being summed in the cost function to give a total error. This is carried out for all the vectors, and the vector with the lowest error is then applied in the next interval.

The scaling factors are chosen based on the following rationale: the factor for the current tracking does not affect the average volt seconds applied within an interval, providing that the residual voltage error is less than the lowest capacitor voltage. This condition can be enforced within the algorithm by specifically excluding vectors for which this condition is not true. The total applied volt seconds is always precise due to the residual voltage being applied via the symmetrical PWM.

The remaining scaling factors can be tuned by experimentation. Firstly a reasonable scaling factor for the voltage balancing error is chosen to give an error with the same order of magnitude as the current tracking error. If the switch utilisation scaling factor is set to zero, the voltage balancing will dominate the cost function and give the tightest control over capacitor voltage ripple. A non-zero setting for the switch utilisation scaling factor reduces the device switching. As this value increases at some point the voltage ripple on the capacitors will become unacceptable. The maximum capacitor voltage ripple will be dependent on the chosen capacitors and the effect of voltage ripple on their lifetime. Further manipulation of the scaling factors is discussed in Section VI.

IV. Simulation results

A simulation of the scheme has been implemented in Saber®, and is very accurate and comprehensive. It completely simulates the H-bridge phase legs, the start-up sequencing and all control loops. It is a multi-mode simulation, with the control implemented digitally with the timing as per the experimental system. The key control algorithms are implemented as 'C' DLLs, and this code is also used in the actual experimental system.

Fig. 2 shows waveforms for a transient condition within the H-StatCom system. From 0.45s to 0.55s the H-StatCom is supplying inductive VARS. At this point a transient from 4KVARS inductive to 4KVARS capacitive occurs. Fig. 2 shows the 'a' phase H-StatCom current (bottom), line voltage (top), stack voltage (top) and the nine capacitor voltages for phase 'a' (middle).

The system has a high bandwidth, with the change of state occurring in one control interval ($400\mu s$). This achieves the same performance as the deadbeat control previously implemented on this system [8].

The capacitor voltages all have the normal 100Hz ripple component present in H-StatCom systems, however the deviation from the mean DC value can be increased by penalisaton of switching transitions in the cost function. The MPC controller allows increased voltage excursions away from the mean DC value. This is due to the simultaneous minimisation of the switching transitions. A detailed discussion regarding the optimality of the trade-offs between the number of switching transitions and the increased ripple in the capacitor voltages is provided in Section VI.

Fig. 3 demonstrates the current tracking performance of an MPC scheme similar to that developed in [6]. The Cortes implementation, in [6], of the MPC algorithm limits the subspace of switching combinations to only allowing progression of the voltage, in the next control interval, to an adjacent vector. The waveforms show that the current tracking is good when the system is in steady state. However under transient conditions it is possible that the current experiences an overshoot as seen in Fig. 3. The overshoot occurs as a result of the voltage increasing positively to drive the current to it's new reference value, however once the current reaches the reference, the voltage vector ideally needs to have a negative polarity. Due to the limited subspace evaluation, the voltage takes a finite period to reach the ideal vector and therefore current overshoot occurs. This differs from the results in Fig. 2 which show that by evaluating the entire set of switching combinations the dynamic performance is only limited by the control frequency and DC capacitor voltage.

V. Experimental Results

In order to validate the simulation studies, the 'C' code dll used in the Saber simulation was slightly modified for operation in the real-time control environment of a low voltage (415VAC) 19 level H-bridge StatCom. The StatCom used to produce the experimental results is a scaled model of an 11kV StatCom. It has 9 H-bridges per phase, with each H-bridge designed with MOSFET power devices. The phase legs are Wye connected. A block diagram of the experimental system appears in Fig. 4. One can see that it is implemented as a multi-processor system, with individual processors implementing the control for each of the phase legs. These phase leg processors are responsible for switching in the desired capacitors and applying the PWM. The desired switching vectors which are passed to the phase leg controllers are developed in the MPC algorithm, which is implemented in a central Pentium PC.

Fig. 5 shows the actual 'a' phase H-StatCom current and the reference current on the top plot, and the nine capacitor voltages for phase 'a' for the start-up condition within the H-StatCom system on the bottom plot. At 0.125s the H-StatCom capacitors have been charged sufficiently and the control scheme begins

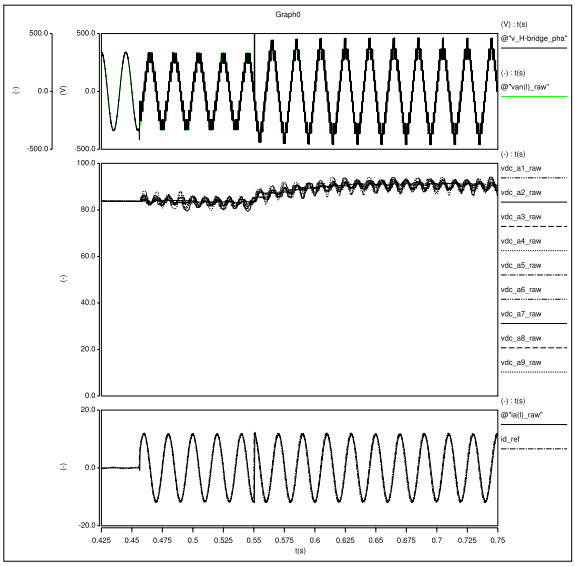

Figure 2. Current, stack voltage and capacitor voltage waveforms

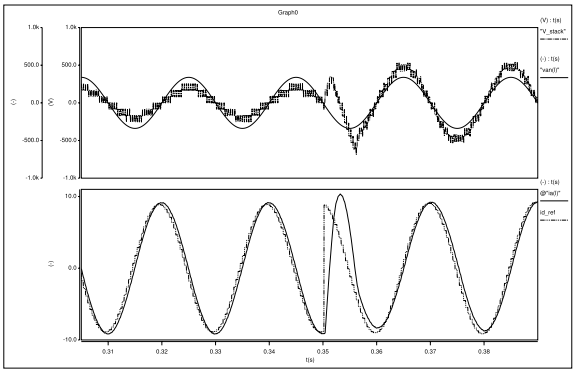

Figure 3. H-StatCom current and voltage waveforms under the condition of a limited subspace of switching combinations

producing currents to supply 1.3KVARs inductive. It can be seen in Fig. 5 that the system achieves a good current tracking performance with tight control over the capacitor voltages. The capacitor voltage ripple is similar to that achieved by a previous system described in [8]. This is due to the fact that the switch utilisation penalty was set to zero to obtain these results, and therefore the MPC algorithm is selecting the same vectors as in [8], which optimise the control of the capacitor voltages.

The top graph in Fig. 5 shows that there is a small error in the resultant H-StatCom current when compared to the reference current. This is due to the cumulative effect of the diode and switch voltage drops on the current tracking performance. This

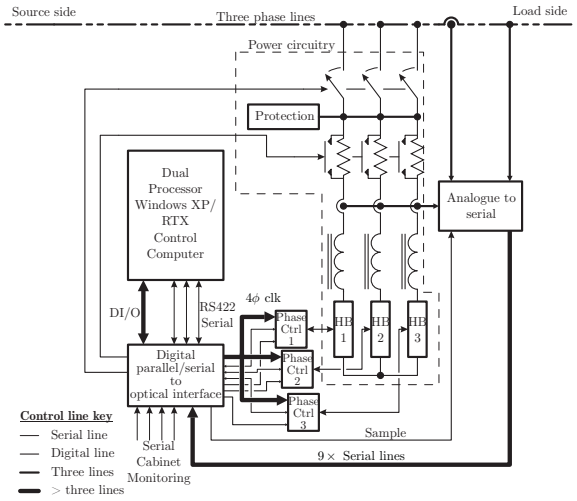

Figure 4. Block diagram of the experimental system.

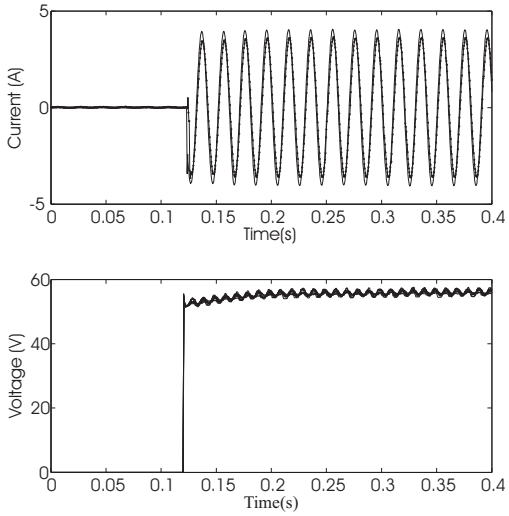

Figure 5. Experimental H-StatCom current and capacitor voltage waveforms

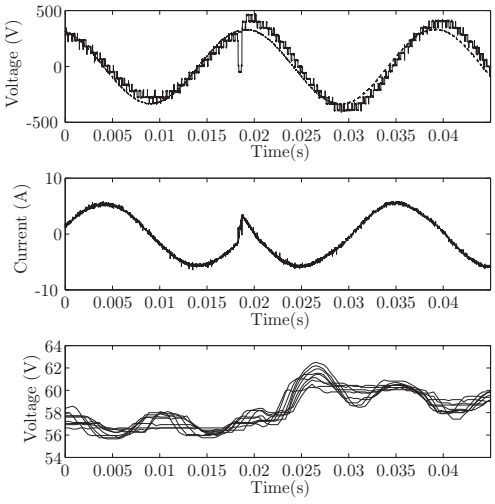

Figure 6. Experimental H-StatCom current, voltage and capacitor voltage waveforms

effect is exacerbated in any H-StatCom system which uses a predictive current controller, such as that employed in the model within the MPC algorithm. A compensation algorithm has been developed in [10] which uses a feed-forward control structure to modify the applied stack voltage and eliminate the error in the current tracking. With some modification the scheme described in [10] can be integrated into the MPC algorithm by modifying the ideal voltage vector used to evaluate each switching combination. This will be the subject of future work.

Fig. 6 shows waveforms for a transient condition within the H-StatCom system similar to Fig. 2. Initially the H-StatCom is supplying inductive VARS. At approximately 0.02s a transient from 1.3KVARS inductive to 1.3KVARS capacitive occurs. Fig. 6 shows the 'a' phase H-StatCom current (middle), line voltage (top), stack voltage (top) and the nine capacitor voltages for phase 'a' (bottom).

Fig. 6 confirms the high bandwidth of the system with the change in state occurring in one control interval ($400\mu s$). There is excellent correspondence between this experiment and the simulated output shown in Fig. 2.

Fig. 7 shows the re-convergence of the capacitor voltages after the the capacitors have initially undergone unequal charging periods. The MPC algorithm begins operating at approximately 0.04s and within two cycles the voltages converge to the DC mean value. This performance is similar to that achieved previously in [8].

Fig. 8 shows the 'a' phase H-StatCom current, reference current (top plot) and the nine capacitor voltages for phase 'a' (bottom plot) when the H-StatCom is supplying 1kVAR inductive. The switch utilisation penalty within the MPC algorithm

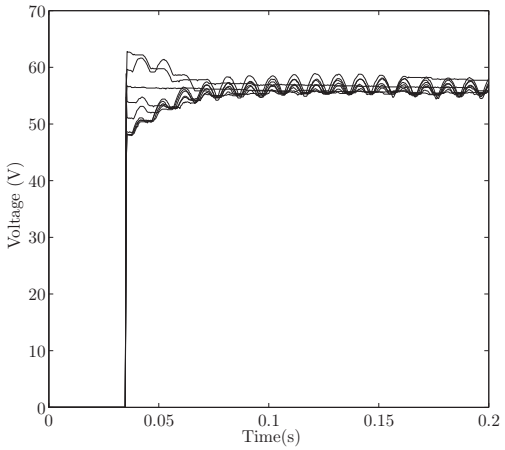

Figure 7. Convergence of the H-StatCom capacitor voltages

has been set at 0.5 to obtain these results. In Fig. 8 it can be seen that the system still achieves good current reference tracking performance with an increased capacitor voltage ripple compared to Fig.s 5 and 6. While the system is still achieving capacitor voltage balancing, by penalising the number of switch transitions the MPC algorithm is able to optimise the switching losses at the expense of capacitor voltage ripple.

To quantify the amount of optimisation which can be achieved by employing this control structure, varying penalties were applied to the switching component of the MPC cost function over a 3.2s period. The results of this experimentation are shown in Table I. These results are compared to the traditional modulation schemes for a H-StatCom in Section VI.

VI. Discussion

It is possible to investigate the trade-off between harmonic performance and switching losses for the MPC scheme. This can be done in various ways however many commercial H-StatComs use the switching frequency per component as the basis for their design choice [11]. Traditionally the best trade-off between harmonic performance and switch utilisation is achieved using Phase Shifted Carrier Pulse Width Modulation (PSC-PWM). The authors have developed a H-StatCom simulation which implements PSC-PWM. This simulation is similar to the implementation in [9] with the notable omission of the PI loops which control the individual capacitor voltages. Instead, the author's PSC-PWM simulation assumes inherently balanced individual capacitor voltages i.e. ideal voltage sources replacing the H-bridge capacitors. This simulation provides the theoretical values of total harmonic distortion which can be achieved within

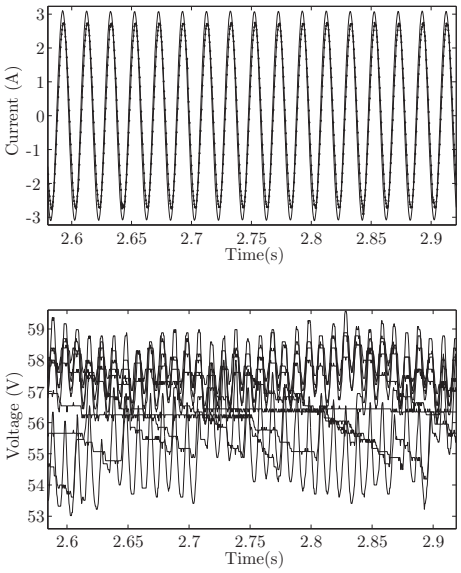

Figure 8. Experimental H-StatCom current and capacitor voltage waveforms with an increased switching penalty

the H-StatCom system.

To gain similar harmonic performance to that of the MPC scheme described in this paper, the PSC-PWM simulation requires a carrier frequency of 250Hz [12]. For PSC-PWM each switching device will undergo two switching transitions per period of the carrier waveform, this is due to the fact that PSC-PWM switches in each bridge during every period of the carrier waveform. This means the total switching transitions per component for a 3.2s period of time will be 1600.

The number of transitions as a function of MPC switching penalty is shown graphically in Fig. 9. The number of transitions for a PSC-PWM scheme is shown to provide a comparison.

Remark 2: To provide a comparison between the author's scheme and PSC-PWM the voltage ripple, and it's effect on capacitor lifetime, must also be considered by the system designer. With identical H-StatCom currents, the implementation of PSC-PWM will result in a different capacitor voltage ripple to that of MPC. This is due to the differing pulse widths which result when using PSC-PWM. When creating a large stack voltage i.e. capacitive currents, the pulse widths for all bridges become larger and therefore the ripple will increase. For small stack voltages i.e. inductive currents, the pulse widths for all bridges become smaller and therefore the ripple will decrease. For comparison purposes, the ripple produced in the PSC-PWM

Voltage Balancing Scaling Factor	Switch Utilisation Scaling Factor	Maximum Ripple(V)	Switch Transitions / Component
0.05	0	3.2	3075
0.05	0.1	3.2	2827
0.05	0.2	3.9	2597
0.05	0.3	4.4	2420
0.05	0.4	5	2340
0.05	0.5	5.6	2260
0.05	0.8	6.5	2195
0.05	1.1	9.1	2172

Table I
VOLTAGE RIPPLE AND SWITCH UTILISATION TRADE-OFF

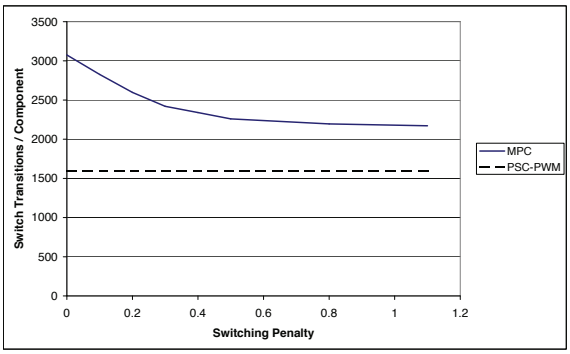

Figure 9. Switching transitions as a function of cost function coefficient

scheme can be considered to be similar to that of the case of zero switch utilisation penalty. This is the case in which the only component of the ripple is the normal 100Hz component traditionally seen in H-StatCom systems. ■

The experimental results show that the MPC algorithm can significantly reduce the switching transitions up to a certain point. The shape of the plot shown in Fig. 9 indicates that as the switching penalty increases beyond 0.5 the rate at which the transitions reduce starts to decrease. The system is reaching a limit imposed by the fact that a minimum number of transitions need to occur to allow creation of the basic shape of the voltage waveform. The MPC algorithm must switch in enough capacitors so that the PWM can create the extra volt seconds to accurately track the reference current. As only one bridge is PWM'd a minimum number of capacitors must be switched in to create the majority of the output stack voltage, as the sinusoidal shape of the waveform progresses.

These results have important implications for the trade-offs between schemes based on symmetrical PWM and phase-shifted carrier PWM schemes. The switching frequency per component of the MPC scheme was not shown to be less than that of PSC-PWM. However, when considering the harmonic degradation of the practical implementation of PSC-PWM schemes [13], the use of MPC will allow the performance of symmetrical PWM schemes to exceed that of PSC-PWM, in some H-StatCom applications. Therefore, it is proposed that with the ease of implementation of symmetrical PWM this technique will begin to gain wider acceptance for use in H-StatComs above a certain level number.

It has been shown that MPC allows a trade-off between capacitor voltage ripple and the number of switching transitions. The MPC algorithm can be modified to further optimise this trade-off and reduce the voltage excursions without significantly increasing the switching transitions. This involves modifying the model of the voltage balancing used within the cost function. Instead of only penalising the position of the proposed capacitor voltage, when compared to an ideal vector, the relative voltage difference between each capacitor and the mean DC value can also be penalised. This should decrease the number of voltage excursions outside the normal 100Hz ripple. To further optimise the trade-off, the scaling factors within the cost function can be changed dynamically depending on where in the voltage and current waveform the next control interval resides. These techniques will be the subject of future work.

VII. CONTRIBUTIONS & CONCLUSIONS

This paper presents a new MPC control scheme for a H-StatCom which achieves simultaneous optimisation of the current reference tracking, voltage balancing and switch utilisation. This algorithm is integrated with a novel hybrid PWM and MPC modulation scheme to implement a current controller. Comprehensive simulation and experimental results showing the performance of the algorithms have been presented. Future work will aim to optimise the trade-off between capacitor voltage ripple and switch utilisation which will further increase the performance of symmetrical PWM relative to the traditional phase shifted carrier modulation schemes.

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